IN THE UNITED STATES PATENT AND TRADEMARK OFFICE Group Art Unit: 2812 Examiner: Unknown e Patent Application of Applicant Liu Guo LIN **SECOND** 10/023,739 Application No.: **PRELIMINARY AMENDMENT** December 21, 2001 Filed STRUCTURE OF For SEMICONDUCTOR ELECTRONIC 26694 DEVICE AND METHOD OF MANUFACTURING THE SAME PATENT AND TRADEMARK OFFICE 32014-177429 Attorney Docket: **Assistant Commissioner for Patents**

Sir:

Prior to examination, please amend the application as follows:

IN THE SPECIFICATION:

Washington, D.C. 20231

Please substitute the attached pages 15-21 for original pages 15-20.

IN THE CLAIMS:

Please amend claims 5 and 6 as follows:

5. (Amended) A method of manufacturing a semiconductor electronic device, comprising the following steps:

a step for forming a gate electrode of a field effect transistor over a substrate;

a step for forming first side walls over side walls of said gate electrode on a selfalignment basis respectively;

a step for performing over etching and etching edges of said first side walls by using trenching effects at the edges of said first side walls until said substrate is exposed;

a step for subjecting the exposed substrate to thermal oxidation to thereby form an oxide film substantially identical in quality to a gate oxide film; and

a step for forming second side walls over side walls of said first side walls; and wherein said respective steps are successively executed.

6. (Amended) A method of manufacturing a semiconductor electronic device, comprising the following steps:

a step for forming a gate electrode of a field effect transistor over a substrate;

a step for forming first side walls over side walls of said gate electrode on a selfalignment basis respectively;

a step for performing over etching and etching edges of said first side walls by using trenching effects at the edges of said first side walls until said substrate is exposed;

a step for further etching said exposed substrate;

a step for forming an oxide film on said exposed substrate substantially identical in quality to a gate oxide film by thermal oxidation; and

a step for forming second side walls over side walls of said first side walls; and wherein said respective steps are successively executed.

Claim 10 was previously amended with the Preliminary Amendment filed December 21, 2001 as follows:

10. (Previously Amended) The method as claimed in claim 5, wherein said substrate is an SOI substrate or an Si substrate.

Please add claims 15 - 17 as follows:

- 15. The method of claim 5, wherein the exposed substrate at the edges of said first side walls is recessed and concave to the surface of the exposed substrate on which the gate electrode of the field effect transistor is formed.
- 16. The method of claim 15, wherein the recessed and concave exposed substrate is at least one of arcuate and rectangular in shape.
- 17. The method of claim 6, wherein the height of said second side walls is less than the height of said first side walls.

REMARKS

This application is a divisional application. Claims 5 and 6 have been editorially amended. Claims 15-17 are added. Further, the specification was amended to place the claims on a separate page, pursuant to 37 C.F.R. § 1.75(h).

In the first Preliminary Amendment, dated December 21, 2001, at the top of page 5 and again on page 10, an amendment to claim 10 was inadvertently marked as being an amendment to claim 5. The remarks in the amendment refer to an amendment to claim 10. Claim 5 was not amended in the first Preliminary Amendment of December 21, 2001.

The attachment to this Amendment entitled "Version with Markings to Show Changes Made" is a marked-up version of the changes made to the claims. The pending claims correspond to Group II, as set forth in the Restriction mailed December 4, 2000 in the parent application, U.S. Patent Application No. 09/663,692, filed September 19, 2000. Applicant hereby requests an action on the merits at the earliest opportunity for claims 5-17 corresponding to Group II.

Respectfully submitted,

Date: Tunuary 23, 2002

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MAS/CJS DC2-344941

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

5. (Amended) A method of manufacturing a semiconductor electronic device, comprising the following steps:

a step for forming a gate electrode of a field effect transistor over a substrate; a step for forming first side walls over side walls of said gate electrode on a self-alignment basis respectively;

a step for performing over etching and etching edges of said first side walls until the exposure of said substrate by using trenching effects at the edges of said first side walls until said substrate is exposed;

a step for subjecting the exposed substrate to thermal oxidation to thereby form an oxide film substantially identical in quality to a gate oxide film; and

a step for forming second side walls over side walls of said first side walls; and wherein said respective steps are successively executed.

6. (Amended) A method of manufacturing a semiconductor electronic device, comprising the following steps:

a step for forming a gate electrode of a field effect transistor over a substrate;

a step for forming first side walls over side walls of said gate electrode on a selfalignment basis respectively; a step for performing over etching and etching edges of said first side walls until the exposure of said substrate by using trenching effects at the edges of said first side walls until said substrate is exposed;

a step for further etching said exposed substrate;

a step for forming an oxide film on said exposed substrate substantially identical in quality to a gate oxide film by thermal oxidation; and

a step for forming second side walls over side walls of said first side walls; and wherein said respective steps are successively executed.

10. (Previously Amended) The method as claimed in claims 5-to-9, wherein said substrate is an SOI substrate or an Si substrate.

invention, will be apparent to those skilled in the art on reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

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